Electronic Version
Stylesheet Version v1.1.1

ELECTRO-STATIC DISCHARGE PROTECTION CIRCUIT

Abstract

An ESD protection circuit including the following: one or more inverters (I1, I2, I3), each of the one or more inverters having an input and an output; an RC network (11) having an output node (RCT), output node (RCT) connected with the input of at least one of said one or more inverters; a clamping device (N3) joined with the output of at least one of one or more inverters (I1, I2, I3); and a feedback device (NKP) in communication with clamping device (N3) and output node (RCT) of RC network (11). An ESD protection circuit according to claim 7, wherein said RC network includes one or more resistors, and one or more decoupling capacitors. In one embodiment, feedback device (NKP) is an NFET and each of one or more inverters (I1, I2, I3) includes a PFET and NFET pair (P0/N0, P1/N1, P2/N2).